

### IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Ug.

**FAIR-07500** 

In re Application of Ara Bicakaci						
Patent No. 6,741,289 B1 Serial No. 09/703,517						
Issue Date: May 25, 2004 Filed: October 31, 2000						
For: TECHNIQUE TO STABILIZE THE CHROMINANCE SUBCARRIER GENERATION IN A LINE-LOCKED DIGITAL VIDEO SYSTEM	1)))))					

Group Art Unit: 2611

Examiner: Victor R. Kostak

SECOND REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR APPLICANT MISTAKE UNDER 37 CFR §1.323

162 North Wolfe Road Sunnyvale, CA 94086 (408) 530-9700

Customer No. 28960

Attn: Decision and Certificate of Correction Branch of the Patent Issue Division

Commissioner for Patents P.O. Box 1450 Arlington, VA 22313-1450

Certificate
AUG 2 5 2004
Of Correction

Sir:

Attached in duplicate is Form PTO-1050 with at least one copy being suitable for printing.

This is a second request for a certification of correction for applicant mistake. The first request was returned with the enclosed copy of the Notification Of Return Of Papers. However, the check in the amount of \$100.00 in accordance with 37 CFR 1.20(a) was not returned with this notification. Therefore, the Applicant is **not** enclosing a new check herewith.

The exact page and line number where the errors are shown incorrectly in the application file are:

In the ASSIGNEE of the PTOL-85B filed April 12, 2004:

Delete "FAIRCHILD SEMICONDUCTORS, INC." and insert --FAIRCHILD SEMICONDUCTOR, INC.--.

The PTO did not rece	eive the follo	
listed item(s)	<u></u>	
	~	

In the DRAWINGS of the Application filed October 31, 2000:

Delete the drawings as filed and replace with formal drawing sheets 1-5.

Respectfully submitted

HAVERSTOCK & OWENS LLP

Dated: 8-(6-04

By:

Registration No.: 32,571 Attorneys for Applicant(s)

# UNITED STATES PATENT AND TRADEMARK OFFICE.

# **CERTIFICATE OF CORRECTION**

PATENT NO. : 4,741,289 B1
DATED : M9425,2004

INVENTOR(S): BICOKCI

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

The title page showing the illustrative figure should be deleted to be replaced with the attached title page.

Drawing sheets, consisting of Figs. 1-7, should be deleted to be replaced with the drawing sheets. consisting of Figs. 1-7, as shown on the attached pages.

On the title page item [73],

Delete "FAIRCHILD SEMICONDUCTORS, INC." and insert –FAIRCHILD SEMICONDUCTOR, INC.--.





#### US006741289B1

# (12) United States Patent

### **Bicakci**

(10) Patent No.:

US 6,741,289 B1

(45) Date of Patent:

May 25, 2004

# (54) TECHNIQUE TO STABILIZE THE CHROMINANCE SUBCARRIER GENERATION IN A LINE-LOCKED DIGITAL VIDEO SYSTEM

<b>(75)</b>	Inventor:	Ara	Bicako	:i, S	San	Jose,	CA	(US)	)
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(73) Assignee: Fairchild Semiconductors, Inc., South

Portland, ME (US)

(\*) Notice: Subject to any disclaimer, the term of this

patent is extended or adjusted under 35

U.S.C. 154(b) by 631 days.

(21) Appl. No.: 09/703,517

(22) Filed: Oct. 31, 2000

### (56) References Cited

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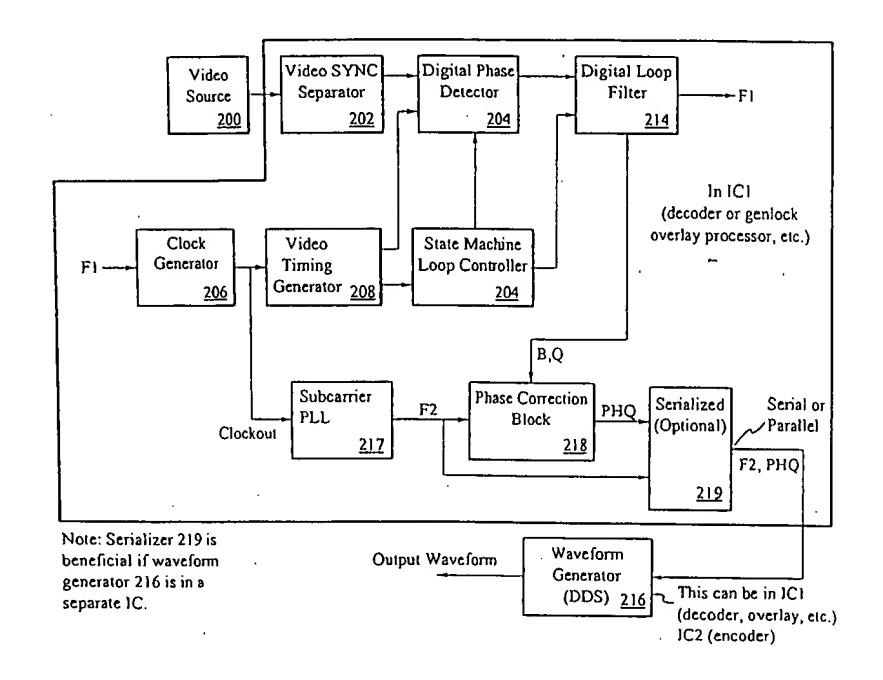
<sup>\*</sup> cited by examiner

Primary Examiner—Victor R. Kostak
(74) Attorney, Agent, or Firm—Haverstock & Owens LLP

### (57) ABSTRACT

A technique to stabilize subcarrier generation in a line-locked digital video system, caused by simultaneous locking of the genlock device causing continuous changing of a shared clock signal, by calculating a time shift occurring in an output waveform, converting the time shift into an equivalent phase shift and sending a corresponding phase correction number to a waveform generator block to correct the time shift, and thus stabilize subcarrier generation.

### 45 Claims, 5 Drawing Sheets



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PATENT NO. :

6,741,289 B1

DATED

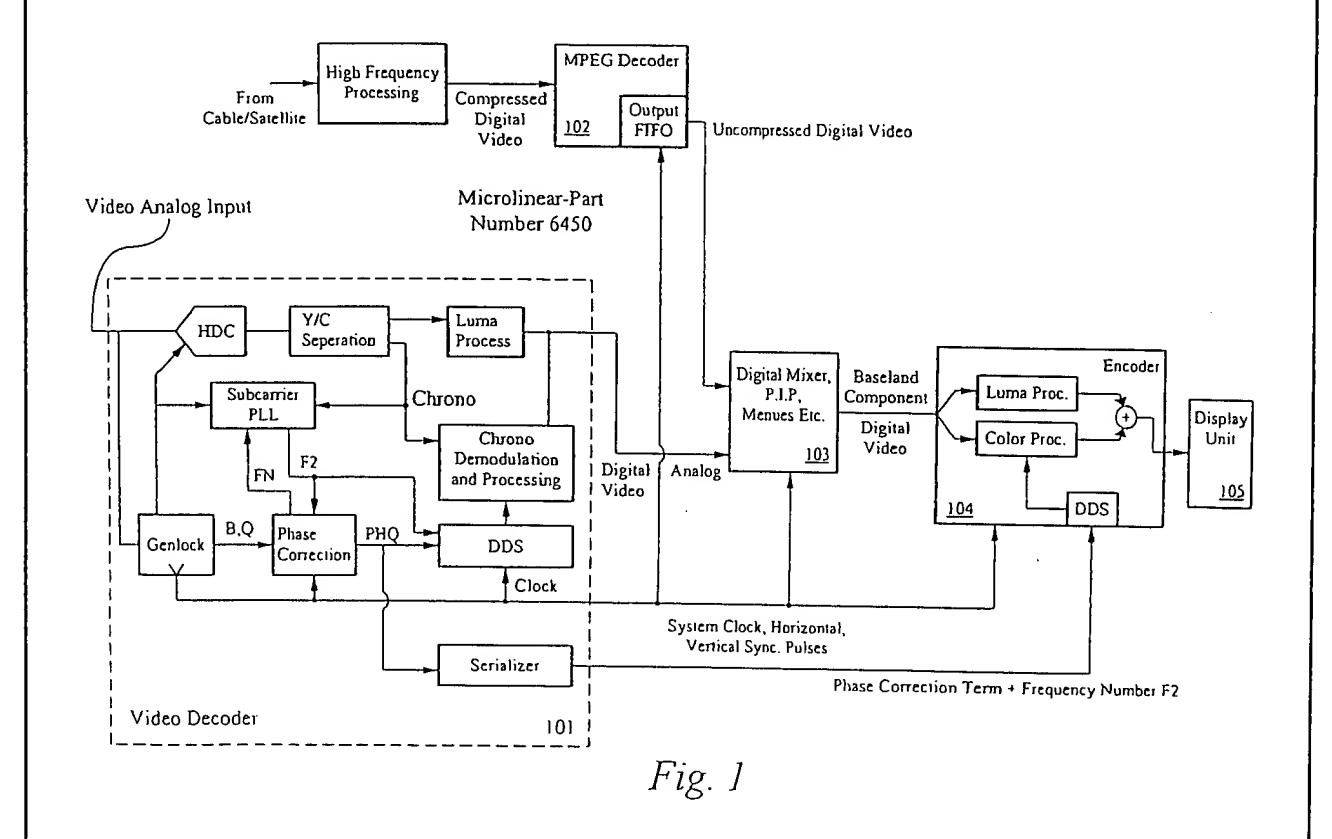
May 25, 2004

INVENTOR(S):

Ara Bicakci

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby correct as shown below:

# IN DRAWING SHEET 1 - REPLACE SHEET 1 AS FILED WITH:



MAILING ADDRESS OF SENDER: HAVERSTOCK & OWENS LLP 162 North Wolfe Road
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6,741,289 B1

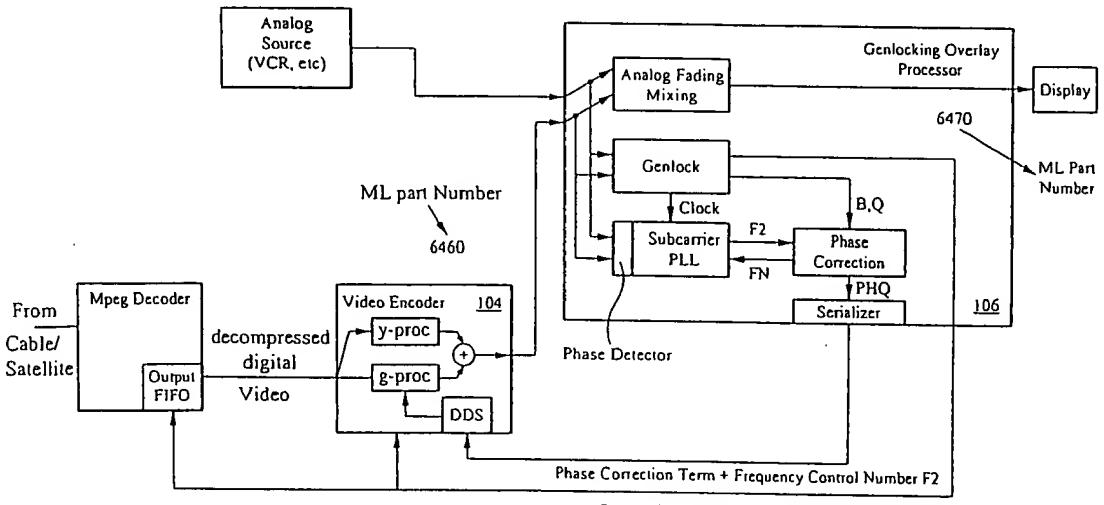
DATED

May 25, 2004

INVENTOR(S): Ara Bicakci

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby correct as shown below:

# IN DRAWING SHEET 2 - REPLACE SHEET 2 AS FILED WITH:



System Clock, Horizontal, Vertical Synchronization Pulses

Fig. 1a

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PATENT NO. : 6,741,289 B1

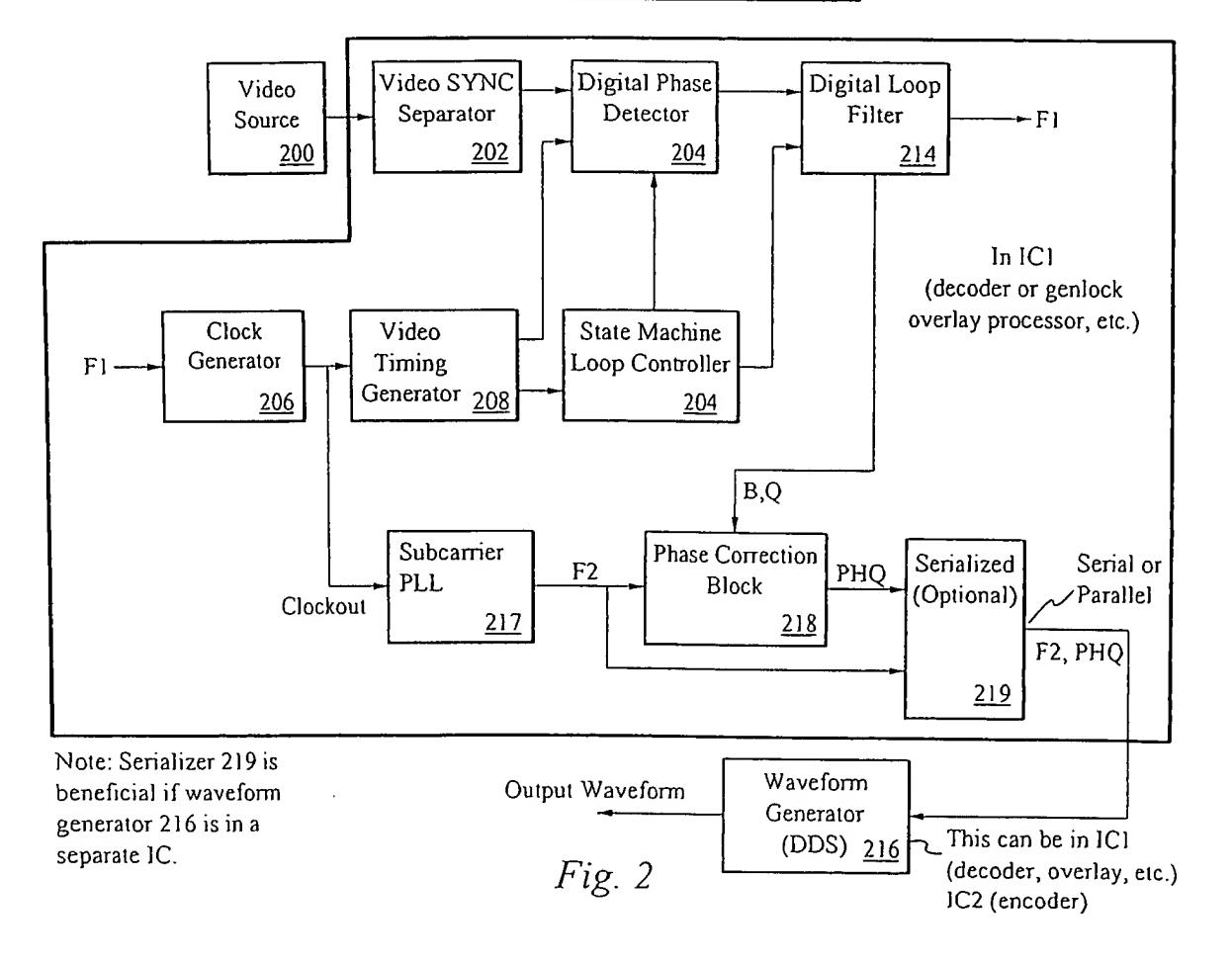
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DATED : May 25, 2004

INVENTOR(S): Ara Bicakci

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### IN DRAWING SHEET 3 - REPLACE SHEET 3 AS FILED WITH:



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DATED

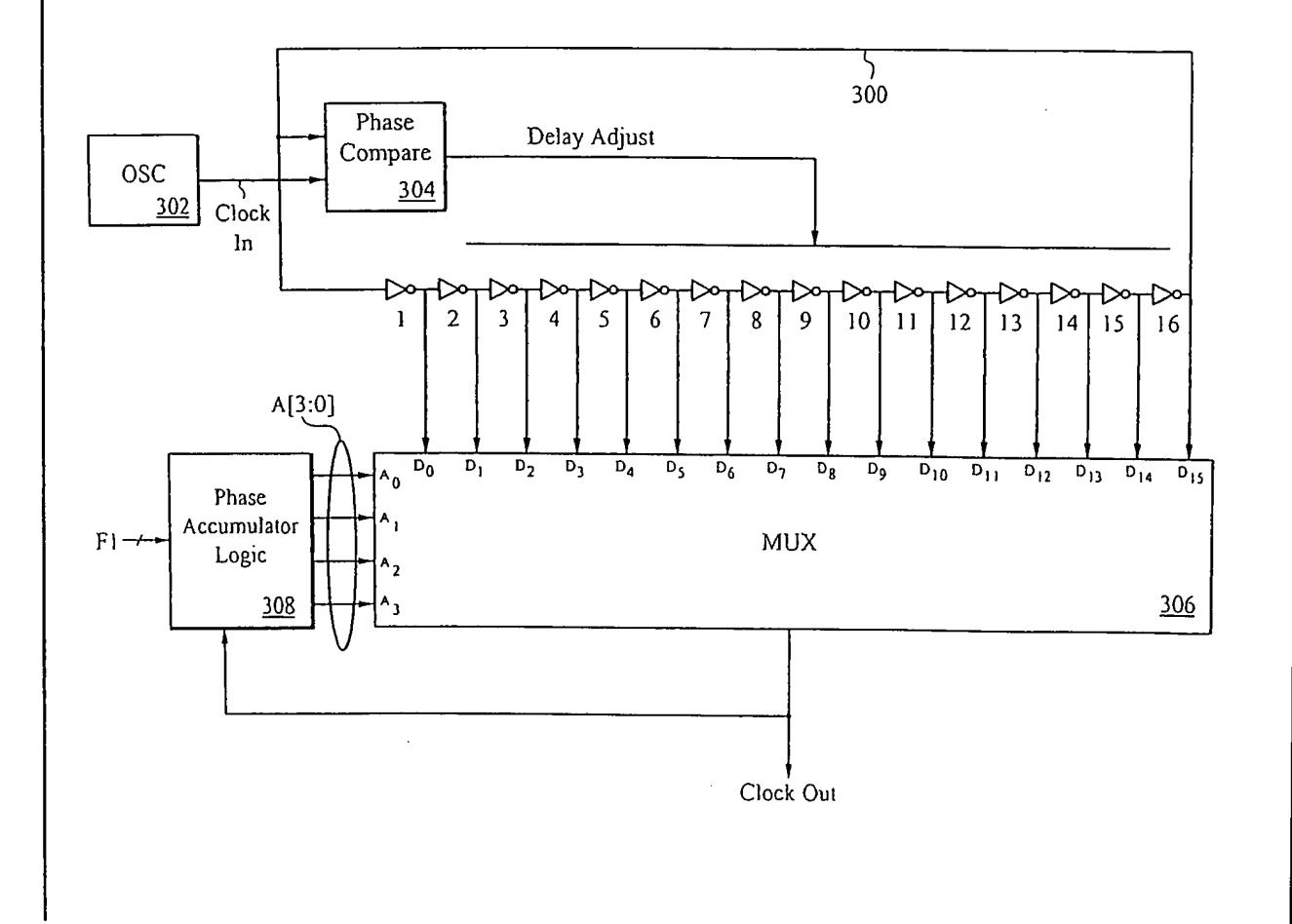
May 25, 2004

INVENTOR(S):

Ara Bicakci

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby correct as shown below:

## IN DRAWING SHEET 4 - REPLACE SHEET 4 AS FILED WITH:



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PATENT NO. :

6,741,289 B1

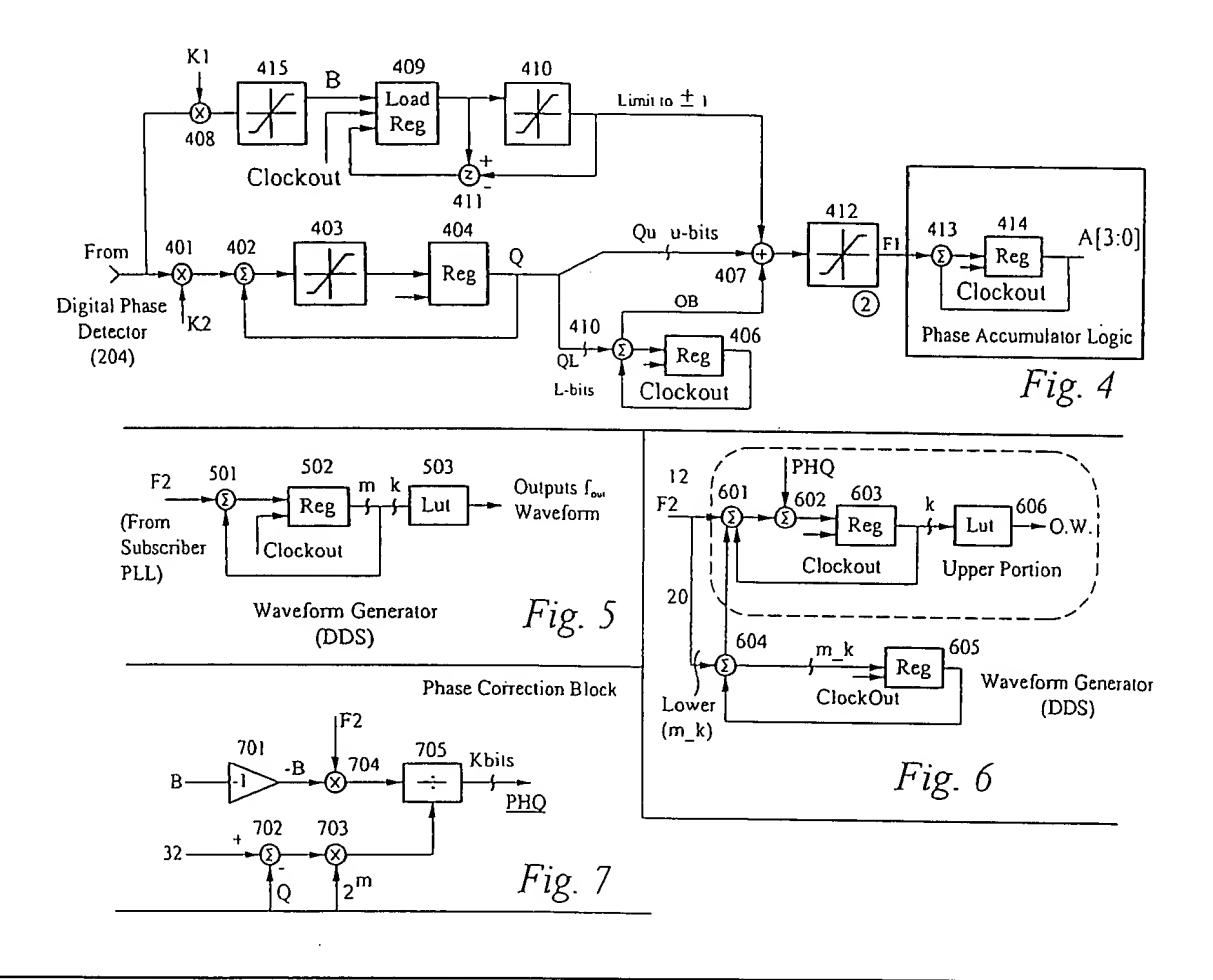
DATED

May 25, 2004

INVENTOR(S): Ara Bicakci

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby correct as shown below:

## IN DRAWING SHEET 5 - REPLACE SHEET 5 AS FILED WITH:



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